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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,431	11/28/2003	Takayuki Kondo	117603	7372
25944	7590	12/12/2005		
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			EXAMINER PEACE, RHONDA S	
			ART UNIT 2874	PAPER NUMBER

DATE MAILED: 12/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary

Application No.

10/722,431

Applicant(s)

KONDO, TAKAYUKI

Examiner

Rhonda S. Peace

Art Unit

2874

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/2/05 *RSP.*
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6,9 and 13-15 is/are rejected.
- 7) ☒ Claim(s) 7,8 and 10-12 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted on 11/28/2003 under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 9, 14, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Leone et al (US 5793909).

Pertaining to claim 1, Leone et al (US 5793909) discloses an optical monitoring and test access module comprising a plurality of circuit blocks **16a** and **18b**, and several optical waveguides **52** and **74**, as well as intra-connective waveguides upon each circuit block **16a** and **18b** which can be seen in Figure 3 (Figure 2-3, column 5 lines 25-39). Note that only block **16a** is shown within Figure 3, for simplicity purposes. These waveguides serve to transmit signals within each of the blocks **16a** and **18b**, as well as in between the blocks **16a** and **18b**. In addition, each circuit block is provided with wavelength division multiplexers **124**, **144**, and **148**, which divide the incoming signal

from input **32** into multiple wavelengths, allowing multiple wavelengths to be transmitted within the block **16a**, as well as from block **16a** to block **18b** (Figures 2-3, column 5 lines 44-50 and column 7 lines 9-20). This module is provided with an electrical backplane **72** and is capable of being mounted upon an integrated circuit chip (column 5 lines 51-56).

With regards to claim 2, Leone et al shows that each of the circuit blocks **16a** and **18b** are electrically connected to one another via electrical backplane **72**, and optically connected to one another via optical backplane **74** (column 5 lines 31-39, Figure 2).

With respect to claims 3-5, a system of several optical waveguides is used in order to create connections between blocks **16a** and **18b**, as previously mentioned. Waveguide **52** is placed upon the top surface of the circuit blocks, as seen in Figure 2, providing a detour route around each of the blocks **16a** and **18b** (column 5 lines 31-39, Figure 2). In addition, a series of waveguides is placed upon the circuit blocks, as it is illustrated with respect to circuit block **16a** in Figure 3, so as to traverse each block (column 5 lines 25-28, Figure 3).

Speaking to claim 6, Leone et al discloses the use of a LED **154**, formed within the circuit block and electrically connected to it, to emit a light of a predetermined wavelength into an intra-block waveguide to be accepted by microcontroller **128** (column 7 lines 1-3, Figure 3). In addition, Leone et al explains the possible use of a photodiode, formed within the circuit block and electrically connected to it, that receives the above-mentioned light of a predetermined wavelength from microcontroller **128**, and modifies it into an electrical signal (column 6 lines 28-33, Figure 3).

Art Unit: 2874

Addressing claim 9, Leone et al teaches the circuit blocks **16a** and **18b** may contain sensors, which may be considered bio sensors, as they are capable of monitoring their surrounding environment with regards to variables such as temperature (column 8 lines 16-34).

As to claims 14 and 15, as previously discussed, Leone et al discloses the use of a photodiode, which receives optical signals from microprocessor **128**, and transforms these optical signals into electrical signals, thereby making the device an electro-optical device (column 6 lines 28-34). In addition, the presence of the electrical backplane **72**, as well as the capability of merging the device with an integrated circuit chip as previously discussed, means this device can also be considered an electronic apparatus (column 5 lines 51-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

Art Unit: 2874

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leone et al (US 5793909).

Addressing claim 13, Leone et al discloses the device as described above. However, the substance of claim 13 calls for duplicating the applicant's device as described in claim 1 in the creation of a larger functional system. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the integrated chip device of claim 1 to create a larger system containing a plurality of integrated chip units, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art (*St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.).

Claim Objections

Claims 7, 8, and 10-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The applicable prior art discussed within this office action do not disclose, nor do they reasonably suggest, the use of light emitting and light receiving elements being in the form of micro-tile shaped elements. As all of the claims indicated above contain

this distinct limitation, it is the opinion of the examiner that this limitation is new over the prior art, and is thereby considered patentable material.

Response to Arguments

Applicant's arguments filed 12/2/2005 have been fully considered but they are not persuasive.

Pertaining to claim 1, the applicant has argued that Leone et al fails to disclose an on-chip optical interconnection circuit, and rather Leone et al simply discloses interconnection modules installed on shelves. However, the recitation "on-chip optical interconnection circuit" has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause (*Kropa v. Robie*, 88 USPQ 478 (CCPA 1951)). Furthermore, the applicant has argues that Leone et al fails to disclose an optical waveguide provided upon an ICC. Jumper fiber **52** and interconnection fiber **74** are considered equivalent to optical waveguides, as both structures transmit an optical signal (column 3 lines 35-38, column 5 lines 42-50). In addition, Leone et al does disclose both fiber equivalents **52** and **74** are provided on an ICC, as these components **52** and **74** are coupled to components **12** and **14**, which are then coupled to the electrical backplane **72**, capable of being provided upon an ICC (column 5 lines 50-56, Fig 2). At this time the examiner notes

that there lies a distinct difference between “an optical waveguide being provided *directly* upon a ICC,” and “an optical waveguide being provided upon a ICC.”

With respect to claims 3-5, the applicant has argued that the Figures 2 and 3 of Leone et al are simply representative schematics, and not a disclosure of an actual arrangement of the Leone et al device. The examiner disagrees with this assertion, as Leone et al discloses that the arrangement between the fiber **52** and the circuit blocks is variable (column 3 lines 35-49). For this reason, the examiner concludes that all arrangements claimed in claims 3-5 are disclosed by Leone et al, as Leone et al has shown there are a number of different ways the fiber can be coupled o the blocks, further showing that the arrangements claimed in claims 3-5 strongly resemble the schematics provided by Leone et al in Figures 2 and 3.

Regarding claim 6, the applicant has argued that the LED **154** disclosed by Leone et al does not emit a light of predetermined wavelength into an intra-block waveguide. However, the wavelength of the LED **154** must be predetermined, as the user cannot control the wavelength it produces by adjusting some variable wavelength producing means. Furthermore, the LED **154** provides a communications test to microcontroller **92**, and therefore must transmit an optical signal into the adjacent waveguide, as can be seen in Figure 3, to do so (column 6 lines 66-67, column 7 lines 1-8).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rhonda S. Peace whose telephone number is (571) 272-8580. The examiner can normally be reached on M-F (8-5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney Bovernick can be reached on (571) 272- 2344. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2874

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Rhonda S. Peace
Examiner
Art Unit 2874


John D. Leo
Primary Examiner